A High-Performance Vector Control of an 11-Level Inverter

José Rodríguez, *Senior Member, IEEE*, Luis Morán, *Senior Member, IEEE*, Jorge Pontt, *Member, IEEE*, Pablo Correa, and Cesar Silva, *Student Member, IEEE*

***Abstract*—This paper presents a switching strategy for multilevel cascade inverters, based on the space-vector theory. The proposed high-performance strategy generates a voltage vector across the load with minimum error with respect to the sinusoidal reference. In addition, it generates very low harmonic distortion operating with reduced switching frequency, without the use of traditional sinusoidal pulsewidth modulation techniques or more sophisticated vector modulation methods.**

***Index Terms*—Digital control, multilevel converter, multilevel inverter, space vector.**

I. Introduction

In THE LAST few years, the power level of industrial processes has increased significantly in order to improve production with minimum cost. This increase caused an important development of high-power medium-voltage adjustable-speed drives (MV-ASDs) [1]. One of the most successful topologies used today in MV-ASDs is the cascade multilevel circuit (CML), which uses several low-voltage cells, each one containing an H-bridge inverter [1], [2]. The classical control of CML inverters uses a standard subharmonic pulsewidth modulation (PWM) control and the phase-shifting technique to achieve a multilevel output voltage [3], [4]. Recently, the space-vector modulation technique has also been successfully applied in CML inverters [5]. With this method, the power switches operate with relative high frequency. A more sophisticated modulation scheme that reduces drastically the switching frequency of the power semiconductors and generates nearly sinusoidal voltages with only fundamental switching frequency, using selective harmonic elimination has been presented in [6] and [7].

This paper presents a control scheme, based on the space-vector theory, which also generates almost sinusoidal voltages with nearly fundamental switching frequency. The operation principle for the proposed modulation scheme is described in the following sections.

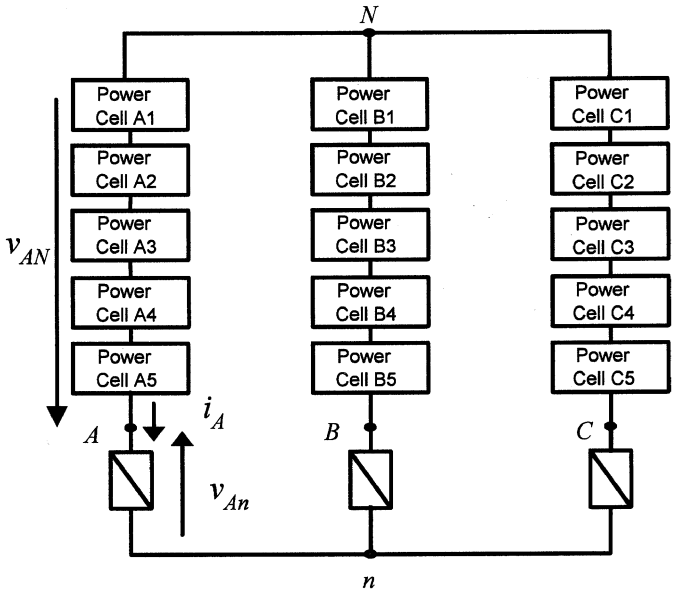

Fig. 1. CML inverter topology.

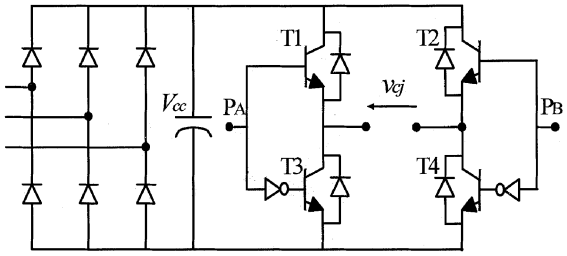

Fig. 2. Cell of the CML inverter.

II. Description of the Inverter

A. Power Circuit

Fig. 1 presents the power circuit topology of a CML inverter with five cells connected in series in each phase. Each cell is composed of a noncontrolled three-phase diode rectifier and a single-phase inverter, as shown in Fig. 2. Each single-phase inverter generates an output voltage with the values $+V_{cc}$, 0, and $-V_{cc}$.

B. Voltages Generated by the CML Inverter

A simplified equivalent circuit for the CML inverter is presented in Fig. 3, where the cells in series in each phase

Manuscript received March 5, 2001; revised May 15, 2002. Abstract published on the Internet September 13, 2002. This work was supported by the Chilean Research Fund (CONICYT) under Projects 1990837 and 1010096 and by the Dirección de Investigación of the Universidad Federico Santa María. This paper was presented at the 3rd International Power Electronics and Motion Control Conference (IPEMC 2000), Beijing, China, August 15–18, 2000.

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Digital Object Identifier 10.1109/TIE.2002.804975

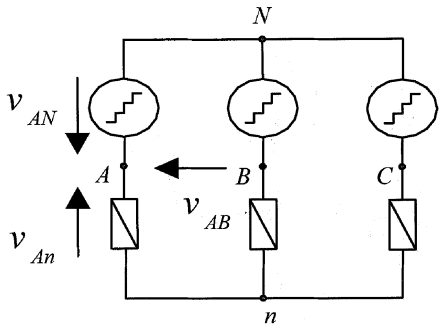

Fig. 3. Simplified equivalent circuit of the CML inverter.

TABLE I
NUMBER OF STEPS IN CML INVERTER VOLTAGES

Number of cells p	Phase-neutral N steps k	Phase-to-phase steps q
1	3	5
2	5	9
3	7	13
4	9	17
5	11	21

are replaced by a voltage source. The number of steps in the phase-to-neutral N and in the phase-to-phase voltages are shown in Table I, for the case in which all the cells per phase have the same dc-link voltage V_{cc}. For example, with one cell per phase, the phase voltage v_{AN} has only three levels: $+V_{cc}$, 0, and $-V_{cc}$. In this connection, the phase-to-phase voltage v_{AB} has five different levels: $+2V_{cc}$, $+V_{cc}$, 0, $-V_{cc}$, and $-2V_{cc}$. The connection of a cell in each phase adds two more levels to the phase voltage v_{AN} and four more levels in the phase-to-phase voltage v_{AB}, as shown Table I.

The number of levels in the phase–neutral voltage v_{AN} is given by

$$k = 2 \cdot p + 1 \tag{1}$$

where p is the number of cells per phase. In addition, the number of steps q in the phase–phase voltage v_{AB} is given by

$$q = 2 \cdot k - 1. \tag{2}$$

An increase in the number of steps in the output voltage produces a reduction in harmonic distortion.

C. Voltage Vectors of the 11-Level Inverter

The vector approach for the three-phase 11-level inverter is defined by the following general expression:

$$\boldsymbol{v}(t) = \frac{2}{3} \cdot (v_{AN}(t) + \boldsymbol{a} \cdot v_{BN}(t) + \boldsymbol{a}^2 \cdot v_{CN}(t)) \tag{3}$$

where v_{AN}, v_{BN}, and v_{CN} are the voltages of terminals A, B, and C with respect to the neutral N and $\boldsymbol{a}$ is the complex operator

$$\boldsymbol{a} = -1/2 + j \cdot \sqrt{3}/2. \tag{4}$$

Each phase can generate 11 different voltages, which correspond to the 11 levels. The three-phase inverter can generate a total of $11 \cdot 11 \cdot 11 = 1331$ space vectors. The representation of the voltage vectors in the complex plane considers that

$$\boldsymbol{v}(t) = v_\alpha + j \cdot v_\beta \tag{5}$$

where v_α and v_β correspond to the components of $\boldsymbol{v}(t)$ in the α and β axes, respectively. These components are given by

$$v_\alpha = \frac{1}{3} \cdot (2 \cdot v_{AN} - v_{BN} - v_{CN}) \tag{6}$$

$$v_\beta = \frac{1}{\sqrt{3}} \cdot (v_{BN} - v_{CN}). \tag{7}$$

There are many inverter phase voltages that generate the same voltage vector. This redundancy property is very useful in optimizing the operation of the inverter. For example, the inverter phase voltages $(5V_{cc}, -2V_{cc}, -4V_{cc})$ and $(4V_{cc}, -3V_{cc}, -5V_{cc})$ are represented by the same vector. However, these inverter voltages produce different common-mode voltages, defined by

$$v_{CM} = \frac{(v_{AN} + v_{BN} + v_{CN})}{3}. \tag{8}$$

It has been shown in MV-ASD systems that high common-mode voltage contributes to motor failures [8]. To reduce this problem, only inverter voltages with minimum common-mode voltage will be used to generate the output vector.

III. VECTOR CONTROL SCHEME

A. Vector Selection Strategy

As shown in (6) and (7), the different values of v_α and v_β are multiples of $V_{cc}/3$ and $V_{cc}/\sqrt{3}$, respectively. To simplify the control, it is advantageous to work with normalized voltage vectors $\boldsymbol{v}'$, given by

$$\boldsymbol{v}'(t) = v'_\alpha + j \cdot v'_\beta \tag{9}$$

where the normalized components are

$$v'_\alpha = \frac{v_\alpha}{(V_{cc}/3)} \quad \text{and} \quad v'_\beta = \frac{v_\beta}{\left(V_{cc}/\sqrt{3}\right)}. \tag{10}$$

By using different normalized voltages, components v'_α and v'_β of the inverter vectors take integer values, as shown in Fig. 4. This figure presents the 311 normalized different voltage vectors generated by the inverter, including, also, the normalized reference vector.

The main idea in the proposed control strategy is to deliver to the load a voltage vector that minimizes the error with respect to the reference voltage vector $\boldsymbol{v}'_{\mathbf{ref}}$. For example, vector $\boldsymbol{v}'_{\boldsymbol{c}}$ generated by the CML inverter has the smallest error with respect to the reference vector $\boldsymbol{v}'_{\mathbf{ref}}$ shown in Fig. 4 and this vector will be generated by the control strategy. The high density of vectors

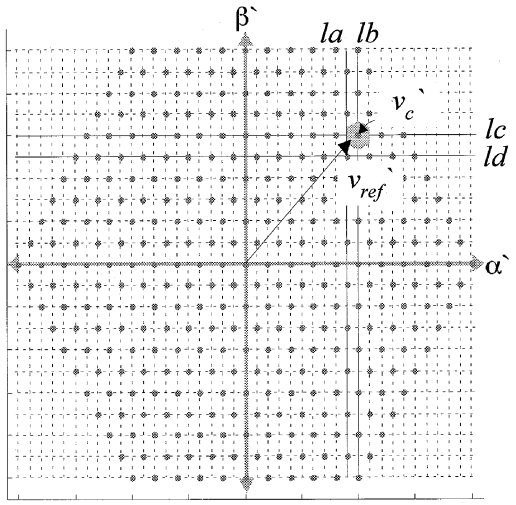

Fig. 4. Normalized voltage vectors generated by the CML inverter.

TABLE II
PULSE GENERATION PER PHASE (EXAMPLE PHASE A)

	Cell 1			Cell 2			Cell 3			Cell 4			cell 5		
v_{AN}	P_A	P_B	v_{c1}	P_A	P_B	v_{c2}	P_A	P_B	v_{c3}	P_A	P_B	v_{c4}	P_A	P_B	v_{c5}
-5 V_{cc}	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	1	$-V_{cc}$
-4 V_{cc}	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	0	0
-3 V_{cc}	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	0	0	0	0	0
-2 V_{cc}	0	1	$-V_{cc}$	0	1	$-V_{cc}$	0	0	0	0	0	0	0	0	0
-1 V_{cc}	0	1	$-V_{cc}$	0	0	0	0	0	0	0	0	0	0	0	0
0 V_{cc}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1 V_{cc}	1	0	V_{cc}	0	0	0	0	0	0	0	0	0	0	0	0
2 V_{cc}	1	0	V_{cc}	1	0	V_{cc}	0	0	0	0	0	0	0	0	0
3 V_{cc}	1	0	V_{cc}	1	0	V_{cc}	1	0	V_{cc}	0	0	0	0	0	0
4 V_{cc}	1	0	V_{cc}	1	0	V_{cc}	1	0	V_{cc}	1	0	V_{cc}	0	0	0
5 V_{cc}	1	0	V_{cc}	1	0	V_{cc}	1	0	V_{cc}	1	0	V_{cc}	1	0	V_{cc}

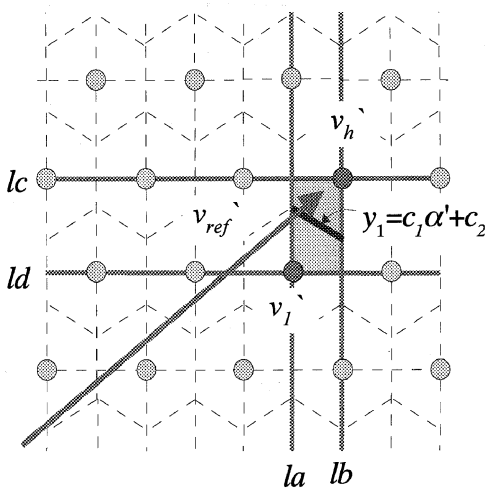

Fig. 5. Representation of the locus with highest proximity to the inverter vector.

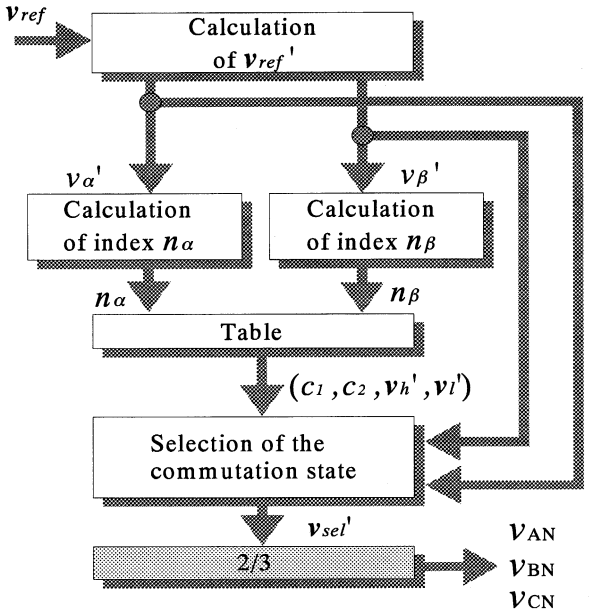

Fig. 6. Block diagram of the control method.

generated by the 11-level inverter will generate small errors in relation to the reference vector. For this reason, it is not necessary to use a complex high-frequency vector modulation scheme using three vectors adjacent to the reference.

The darker hexagon around vector $\boldsymbol{v}'_{\boldsymbol{c}}$ in Fig. 4 represents the locus of highest proximity to this inverter vector. Fig. 5 shows different vectors generated by the CML inverter, with their respective hexagon boundaries of highest proximity area, in dashed lines. The control strategy must determine in which hexagon the reference vector is located, to apply the corresponding voltage vector to the load.

In order to make the appropriate vector selection, the real axis in Fig. 4 is divided into 40 different sections and the imaginary axis is divided into 20 sections. The boundaries la, lb, lc, and ld, shown in Figs. 4 and 5, clearly identify the shaded rectangle, where the reference vector and the nearest inverter vectors are located. The real and imaginary part of $\boldsymbol{v}'_{\mathbf{ref}}$ are used to address a table containing vectors $\boldsymbol{v}'_{\boldsymbol{h}}$, $\boldsymbol{v}'_{\boldsymbol{l}}$, and the equation of trace y_1. The indexes for this table ($\boldsymbol{n}_\alpha$ and $\boldsymbol{n}_\beta$) are easily calculated by the following expressions:

$$\left.\begin{aligned} \boldsymbol{n}_\alpha &= \operatorname{sign}(v'_\alpha)\cdot(\operatorname{ceil}|v'_\alpha|) \\ \boldsymbol{n}_\beta &= \operatorname{sign}(v'_\beta)\cdot(\operatorname{ceil}|v'_\beta|) \end{aligned}\right\} \tag{11}$$

where $ceil(v)$ is defined as the smallest integer greater or equal to v. The next step is to compare the reference vector with the unique trace y_1 in the shaded area of Fig. 5, to select the nearest inverter vector $\boldsymbol{v}'_{\boldsymbol{h}}$ or $\boldsymbol{v}'_{\boldsymbol{l}}$. The trace y_1 is identified by the following equation:

$$y_1 = c_1 \cdot \boldsymbol{\alpha}' + c_2. \tag{12}$$

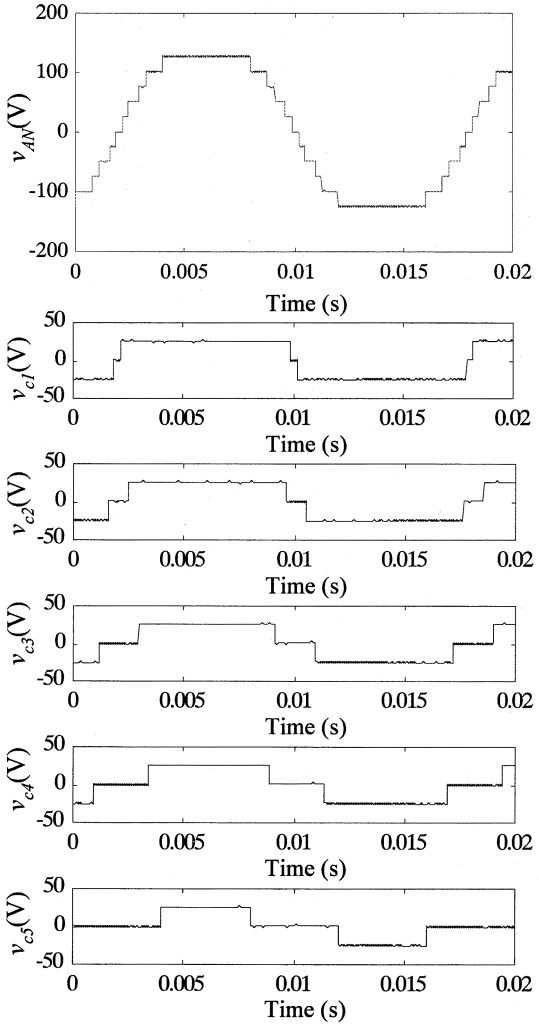

Fig. 7. Cell voltages of a phase, $m = 0.99$.

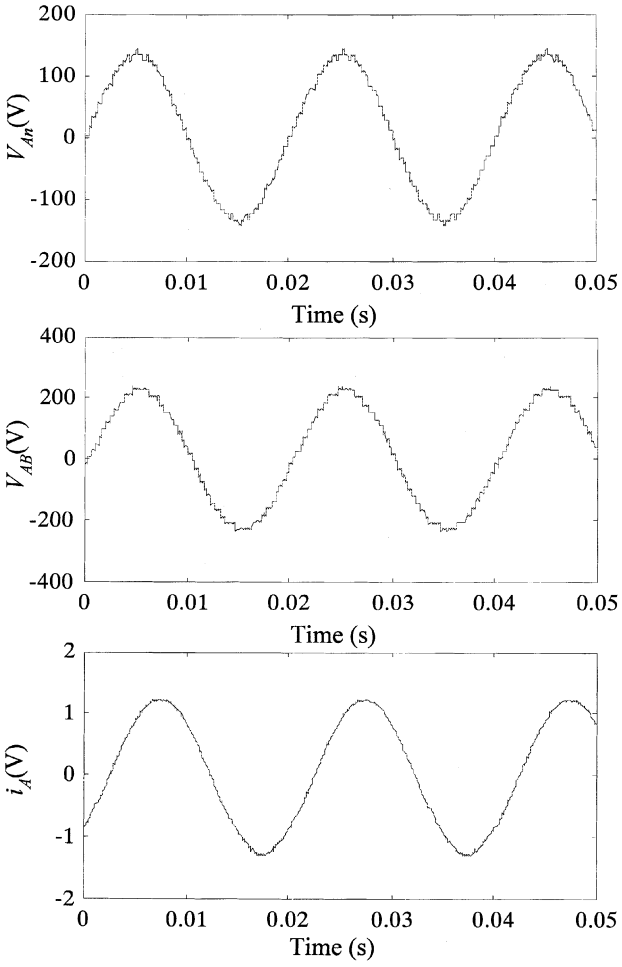

Fig. 8. Different output voltages and current generated by the inverter, with $m = 0.99$.

The coefficients c_1 and c_2 are contained in the same table. Finally, the decision between $\boldsymbol{v}'_{\boldsymbol{h}}$ or $\boldsymbol{v}'_{\boldsymbol{l}}$ is performed utilizing the following relation:

$$\left.\begin{array}{lll} \text{If } v'_\beta > c_1 \cdot v'_\alpha + c_2 & \text{then} & \boldsymbol{v}'_{\boldsymbol{s}} = \boldsymbol{v}'_{\boldsymbol{h}} \\ & \text{else} & \boldsymbol{v}'_{\boldsymbol{s}} = \boldsymbol{v}'_{\boldsymbol{l}} \end{array}\right\} \tag{13}$$

where $\boldsymbol{v}'_{\boldsymbol{s}} = (v_{s\alpha}, v_{s\beta})$ is the selected vector, delivered by the inverter.

B. Generation of the Gating Pulses

The phase–neutral N output voltages v_{AN}, v_{BN}, v_{CN} that must be generated by the inverter are now calculated by using the following equations:

$$v_{AN} = \text{round}\left[\frac{v_{s\alpha}}{3}\right] \cdot V_{cc} \tag{14}$$

$$v_{BN} = \left[\frac{1}{2} \cdot (v_{s\alpha} - v_{s\beta}) \cdot V_{cc} + v_{AN}\right] \tag{15}$$

$$v_{CN} = \left[\frac{1}{2} \cdot (-v_{s\alpha} - v_{s\beta}) \cdot V_{cc} + v_{AN}\right] \tag{16}$$

with the restriction that

$$|v_{AN}|, |v_{BN}|, |v_{CN}| \leqslant p \cdot V_{cc}. \tag{17}$$

The round function in (14) is necessary because the phase voltage v_{AN} can only have integer multiples of V_{cc}. As an illustrative example, when $\boldsymbol{v}'_{\boldsymbol{s}} = (18, 2)$, according to (14)–(16), $v_{AN} = 6V_{cc}$, $v_{BN} = -2V_{cc}$, and $v_{CN} = -4V_{cc}$. The value for v_{AN} is not possible, because the maximum voltage generated by each phase is $5V_{cc}$. To overcome this inconsistency, the value V_{cc} is subtracted from each phase voltage, giving $v_{AN} = 5V_{cc}$, $v_{BN} = -3V_{cc}$, and $v_{CN} = -5V_{cc}$. These new phase voltages generate the desired output voltage $\boldsymbol{v}'_{\boldsymbol{s}}$, because the addition of the same value to the phase voltages does not change the value of the voltage vector.

Table II is utilized to transform each phase voltage in binary control signals $\mathrm{P_A}$ and $\mathrm{P_B}$ used to control the power transistors in each cell. Because each cell has three different states V_{cc}, 0, $-V_{cc}$, only 2 bits are necessary to identify the conduction states of one cell and 10 bits are needed to generate the appropriate phase voltage at the output. For example, when $\mathrm{P_A}$ = "1" and $\mathrm{P_B}$ = "0," transistors T1 and T4 of Fig. 2 are in the ON state and the output voltage of the cell is $V_{cj} = +V_{cc}$. The same Table II is used for phases B and C.

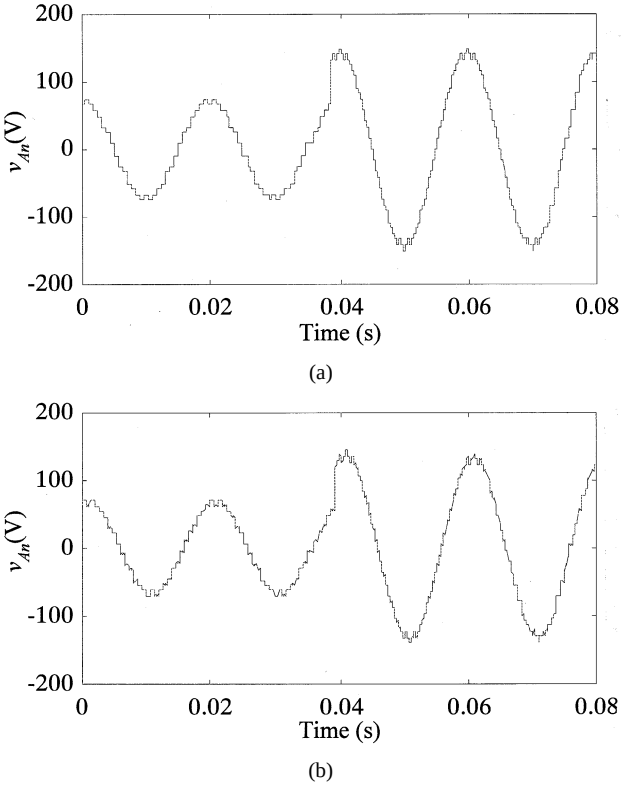

Fig. 9. Response to a reference step change. (a) Simulated. (b) Experimental.

IV. Results

In order to test the proposed control technique, an 11-level multicell converter was constructed. The inverter was controlled using the 16-b fixed-point digital signal processor (DSP) ADMC331 from Analog Devices. The complete algorithm to generate the voltages at the inverter output corresponding to a sample of the reference vector is presented in Fig. 6. This control method has an execution time of 7 (μs).

Fig. 7 shows the voltages generated by the five cells of phase A and the resulting voltage v_{AN} for modulation index $m = 0.99$. It can be observed that each cell works with almost fundamental switching frequency. Fig. 8 presents the steady-state operation of the inverter indicating the phase-to-neutral n voltage v_{An}, the phase-to-phase voltage v_{AB}, and the load current for $m = 0.99$. These figures clearly reveal the 11 levels in the phase–neutral N voltage and the 21 steps in the phase-to-phase voltage in this converter. The load voltage v_{An} is highly sinusoidal with a total harmonic distortion of 4.5%.

The dynamic behavior of the inverter in response to a step change in the amplitude of the reference voltage from $m = 0.5$ to $m = 0.99$ is shown in Fig. 9.

Fig. 10 shows that the total distortion in the phase voltage increases when the modulation index is reduced. This is a typical behavior of all modulation methods. In addition, it is a remarkable fact that the distortion is low and comparable to the distortion observed in multilevel inverters with sinusoidal PWM.

V. Comments and Conclusions

It has been demonstrated that the vector control strategy proposed in this paper originates a high-quality load voltage working with extremely low switching frequency. The vector control strategy is simple and it can be easily implemented in a standard DSP motor controller. The complete control algorithm with the ADMC 331 DSP controller has an execution time of 7 (μs).

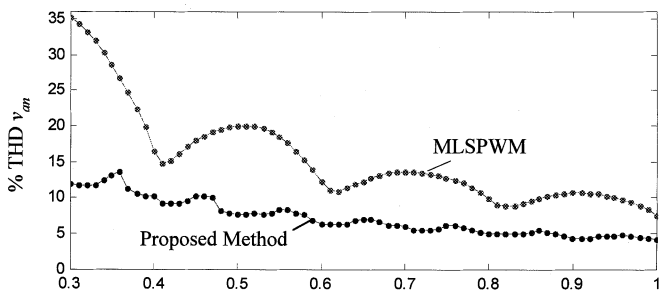

Fig. 10. Load voltage THD for different modulation indexes in the proposed method and the multilevel sinusoidal PWM strategy (MLSPWM).

References

[1] D. Rendusara, E. Cengelci, P. Enjeti, V. R. Stefanovic, and W. Gray, "Analysis of common mode voltage—'Neutral shift' in medium voltage PWM adjustable speed drive (MV-ASD) systems," in *Proc. IEEE PESC'99*, vol. 2, 1999, pp. 935–940.

[2] P. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 202–208, Jan./Feb. 1997.

[3] J. Rodríguez, L. Morán, A. González, and C. Silva, "High voltage multilevel converter with regeneration capability," in *Proc. IEEE PESC'99*, vol. 2, 1999, pp. 1077–1082.

[4] R. Teodorescu, F. Blaabjerg, and J. K. Pedersen, "Multilevel converters—A survey," in *Proc. EPE'99*, 1999, CD-ROM.

[5] N. Celanovic and D. Boroyevich, "A fast space vector modulation algorithm for multilevel three-phase converters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1999, CD-ROM.

[6] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 36–44, Jan./Feb. 1999.

[7] S. Siriroj, J.-S. Lai, and T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 2000, CD-ROM.

[8] R. A. Hanna and S. Prabhu, "Medium voltage adjustable speed drives—User and manufacturers experiences," *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 1407–1415, Nov./Dec. 1997.

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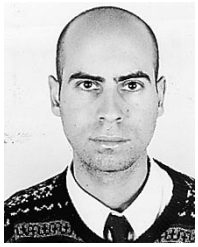

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