A New Modulation Method to Reduce Common-Mode Voltages in Multilevel Inverters

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***Abstract*—This paper proposes a new modulation strategy for multilevel inverters, which selects voltage vectors that generate zero common-mode voltage in the load, working at low switching frequency. Experimental results confirm that the method is highly effective and simple to implement in a modern microprocessor. The voltage distortion (total harmonic distortion), the number of commutations, and the linearity are also studied. Finally, it is concluded that the proposed strategy is highly suited for inverters with a high number of levels.**

***Index Terms*—Common-mode voltage, multilevel converter, multilevel inverter, space vector.**

I. Introduction

THE problem of common-mode voltage generation in inverter-fed ac machines has been extensively studied in the last number of years [1]–[3]. It has been shown that in medium-voltage adjustable-speed drive applications, which are associated with critical processes, the common-mode voltage is an important issue to consider [2], [4].

Common-mode voltages are associated to shaft voltages and circulating leakage currents through parasitic capacitances between the motor windings, the rotor, and the frame. The amplitude and number of these current spikes is determined by the dv/dt and the number of commutations present in the common-mode voltage. These current spikes can cause premature motor bearings failures and electromagnetic interference (EMI) [3]. Some solutions are based on additional hardware, like filters [2], [5], and other methods based on more advanced modulation strategies which avoid the generation of common-mode voltages are applicable in the area of multilevel inverters [4], [6]. However, these methods work with high switching frequency.

The principle of only zero common-mode switching states application is also exploited in the work presented here. In addition, the modulation technique used is characterized by a low switching frequency, witch also helps to reduce the common-mode current spikes problem. This modulation has been presented previously by the authors in [7], where a multilevel inverter has been shown to operate with almost fundamental switching frequency, maintaining good quality voltage and current waveforms. Here, the imposition of zero common-mode voltage is added to the modulation technique, effectively reducing the number of possible switching states available. Nevertheless, it will be shown that, for multilevel inverters of a high number of levels (seven or higher), the reduction on the switching states does not affect significantly the quality of the resulting line currents while successfully eliminating the common-mode voltages.

This paper presents a control method, for high-level multilevel inverters, based on the space-vector theory, which completely eliminates common-mode voltages. The following sections of the paper present the modulation algorithm and experimental results obtained with seven-level and 11-level inverters.

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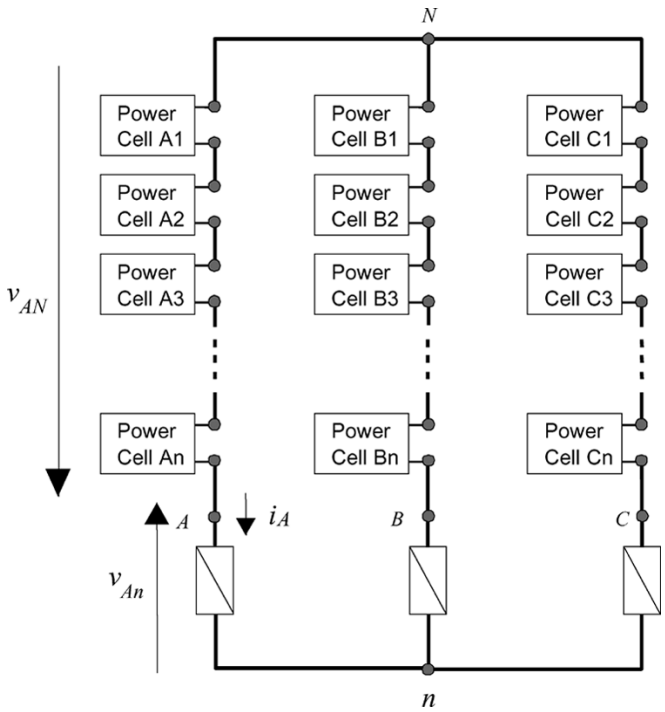

Fig. 1. Power circuit of the cascade multilevel (CML) inverter.

II. Power Circuit Topology

Fig. 1 presents a general diagram for the power circuit of a multilevel inverter, which is applied in medium-voltage drives.

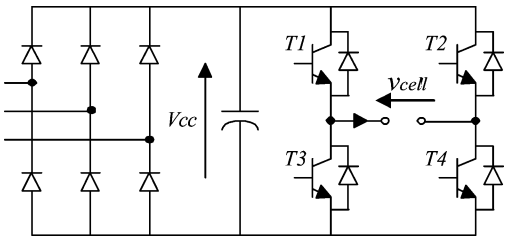

Fig. 2. Power circuit of a single cell.

Each cell is composed of a noncontrolled three-phase diode rectifier and a single phase H-type inverter, as shown in Fig. 2. Each single-phase inverter generates an output voltage with three possible values: $+Vcc$, 0, and $-Vcc$.

III. Common-Mode Voltage Generation in Vector Modulation Schemes

Three-phase inverter output voltages can be represented by a space vector in a x–y plane using the following transformation:

$$\boldsymbol{v} = v_x + j \cdot v_y = \frac{2}{3} \cdot (v_{AN} + \boldsymbol{a} \cdot v_{BN} + \boldsymbol{a}^2 \cdot v_{CN}) \quad (1)$$

where v_{AN}, v_{BN}, and v_{CN} are the voltages of terminals A, B, and C with respect to the neutral N and $\boldsymbol{a}$ is the complex operator

$$\boldsymbol{a} = \frac{-1}{2} + j \cdot \frac{\sqrt{3}}{2}. \quad (2)$$

Equation (1) can be expressed as a function of their real and imaginary components

$$\begin{aligned} \boldsymbol{v} &= v_x + j \cdot v_y \\ &= \frac{1}{3} \cdot (2 \cdot v_{AN} - v_{BN} - v_{CN}) + j \cdot \frac{1}{\sqrt{3}} \cdot (v_{BN} - v_{CN}). \end{aligned} \quad (3)$$

Considering the inverter of Fig. 1 with three cells per phase (seven-level), each phase can generate seven different voltages. Thus, the three-phase inverter has a total of $7 \cdot 7 \cdot 7 = 343$ different output voltages v_{AN}, v_{BN}, and v_{CN}. These voltages generate 127 different voltage vectors represented by dots in Fig. 3. The production of space vectors with different combinations of phase voltages is known as redundancy. This redundancy property is due to the existence of zero-sequence components in the phase voltages. For example, voltages $(v_{AN}, v_{BN}, v_{CN}) = (3Vcc, -Vcc, -2Vcc)$ and $(v_{AN}, v_{BN}, v_{CN}) = (2Vcc, -2Vcc, -3Vcc)$ generate the same vector, but the second set of voltages is clearly unbalanced ($v_{AN} + v_{BN} + v_{CN} \neq 0$).

The common-mode voltage is defined as [1], [4]

$$v_{cm} = \frac{1}{3} \cdot (v_{AN} + v_{BN} + v_{CN}). \quad (4)$$

Considering this definition, it is possible to find vectors generated by three phase voltages, which produce zero common-mode voltage. These vectors are represented by a dot within a circle in Fig. 3 and are obtained with balanced phase voltages.

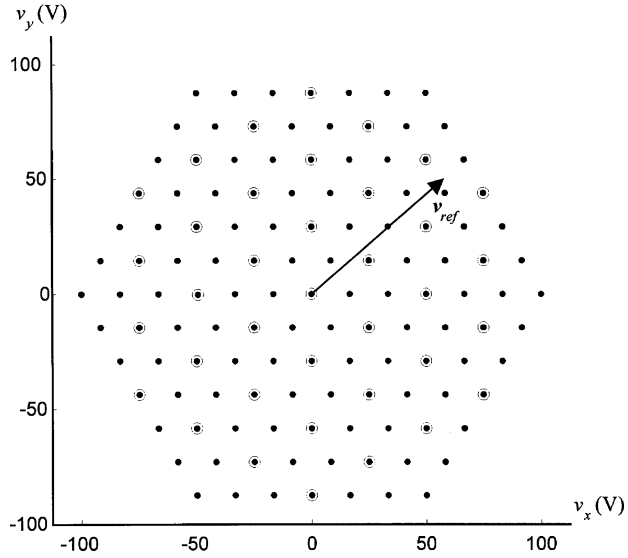

Fig. 3. Voltage vectors of a seven-level inverter, including vectors with $v_{cm} = 0$ ($\odot$).

There are many papers that address this problem using only vectors with zero common-mode voltage for the modulation of the commanded voltage [4], [6], however, none of them have been developed in the context of low commutation frequency. In this paper, the high density of vectors, inherent in multilevel inverters with a high number of levels, is exploited to reduce the number of commutations.

IV. Multilevel Sinusoidal Pulsewidth Modulation (MLSPWM)

The classic PWM method based on the comparison between a sinusoidal and carrier signal is commonly used in industrial cascaded inverter topologies [8] and, for this reason, it will be used as a reference to make an assessment with the proposed control strategy.

The MLSPWM method has in one phase C_n cascaded cells with their carriers shifted by an angle $q = 360°/2C_n$, being compared with respect to the same reference signal in order to obtain a $2C_n + 1$-level phase-neutral N output voltage. The resulting load voltage has a sinusoidal multistep PWM waveform shown in Fig. 4, for a seven-level inverter. Fig. 5 shows that this modulation method generates an important amount of common-mode voltages. The high quantity of commutations observed in v_{cm}, which can produce circulating currents through stray capacitances naturally formed in the converter–motor system [3] is especially detrimental.

V. Proposed Modulation Algorithm

The main idea of the proposed strategy is to deliver the nearest voltage vector with respect to the reference vector $\boldsymbol{v}_{\mathbf{ref}}$, choosing only among vectors that generate zero common-mode voltage to the load. The use of only those vectors with zero common-mode voltage reduces the density of vectors available to be applied and, therefore, the method is best suited for multilevel inverters with a high number of levels, i.e., seven levels or more. In order

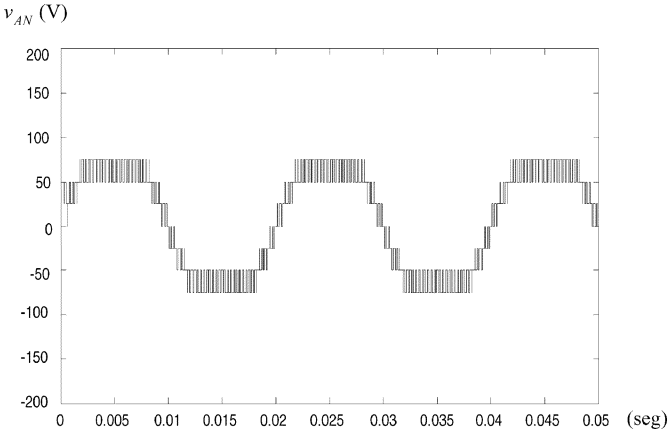

Fig. 4. Seven-level inverter output voltage v_{AN} with MLSPWM (simulation), modulation index $m = 0.9$.

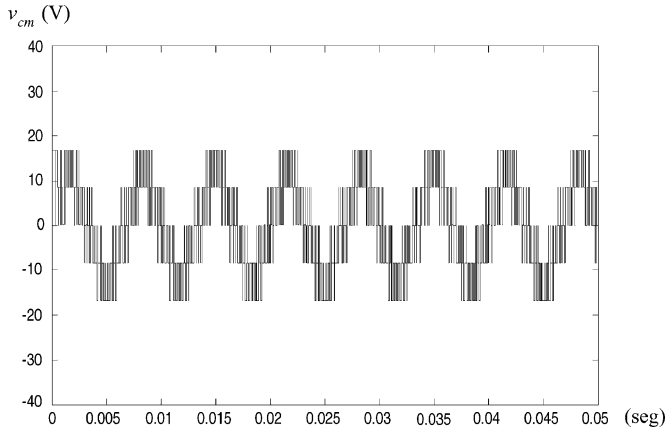

Fig. 5. Seven-level inverter common-mode voltage $v_{\rm c}$ with MLSPWM (simulation), modulation index $m = 0.9$.

to select the appropriate vector with the information of the reference vector, the following simple algorithm has been developed.

Step 1. A transformation is applied to normalize the reference vector $\boldsymbol{v_{\rm ref}} = v_x + jv_y$.

$$\boldsymbol{v'_{\rm ref}} = \frac{v_x}{Vcc} + j \cdot \frac{v_y}{\frac{Vcc}{\sqrt{3}}}. \tag{5}$$

In addition, the transformation of (5) is applied to the position of the candidate space vectors with $v_{cm} = 0$, converting them in to integer values, as can be seen in Fig. 6.

Step 2. There are two vectors with $v_{cm} = 0$ on the corners of each rectangle on the complex plane. These vectors are named $\boldsymbol{v'_h}$ and $\boldsymbol{v'_l}$ for the shaded rectangle where the reference $\boldsymbol{v'}_{\rm ref}$ belongs to (see Fig. 6). The nearest vector is selected comparing the distances of each candidate vector $\boldsymbol{v'_h}$ and $\boldsymbol{v'_l}$ with respect to $\boldsymbol{v'_{\rm ref}}$, using the following equations:

$$d_h = \sqrt{(3\cdot(\mathrm{Re}(\boldsymbol{v'_{\rm ref}}) - \mathrm{Re}(\boldsymbol{v'}_h))^2 + (\mathrm{Im}(\boldsymbol{v'_{\rm ref}}) - \mathrm{Im}(\boldsymbol{v'_h}))^2)} \tag{6}$$

$$d_l = \sqrt{(3\cdot(\mathrm{Re}(\boldsymbol{v'_{\rm ref}}) - \mathrm{Re}(\boldsymbol{v'}_l))^2 + (\mathrm{Im}(\boldsymbol{v'_{\rm ref}}) - \mathrm{Im}(\boldsymbol{v'}_l))^2)}. \tag{7}$$

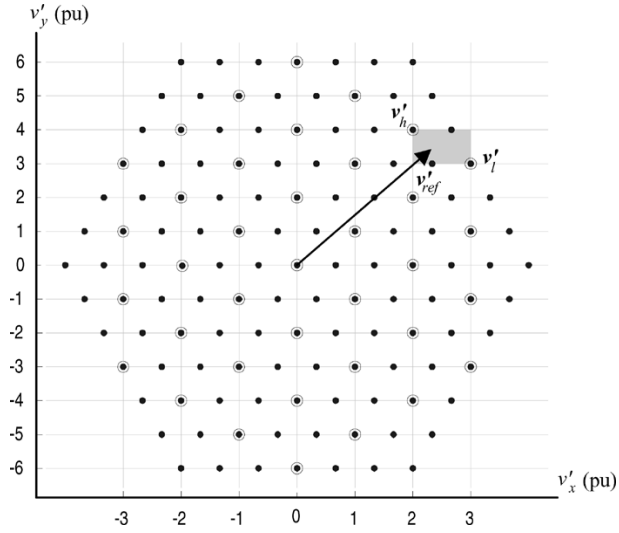

Fig. 6. Normalized space vectors.

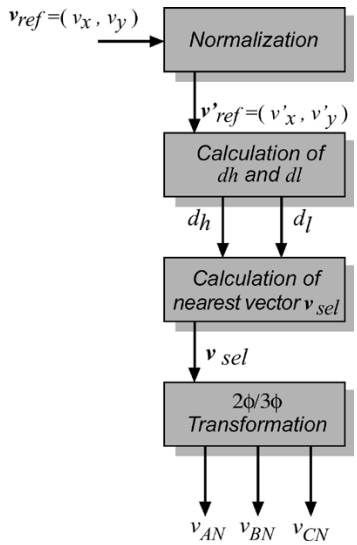

Fig. 7. Control scheme of the proposed strategy.

The decision between $\boldsymbol{v_h'}$ or $\boldsymbol{v_l'}$ is done by:

$$\begin{aligned} \text{if} \quad d_h \le d_l \quad \text{then} \quad & \boldsymbol{v_{sel}} = \boldsymbol{v'_h} \\ \text{else} \quad & \boldsymbol{v_{sel}} = \boldsymbol{v'}_l. \end{aligned} \tag{8}$$

Step 3. An inverse transformation is applied to the selected vector $\boldsymbol{v_{sel}}$ to generate three-phase output voltages with zero common mode voltage. This transformation is given by:

$$\begin{aligned} v_{AN} &= round(\mathrm{Re}(\boldsymbol{v}_{sel})) \\ v_{BN} &= \frac{(\mathrm{Im}(\boldsymbol{v}_{sel}) - 3\cdot\mathrm{Re}(\boldsymbol{v}_{sel}))}{2} + v_{AN} \\ v_{CN} &= \frac{(-\mathrm{Im}(\boldsymbol{v}_{sel}) - 3\cdot\mathrm{Re}(\boldsymbol{v}_{sel}))}{2} + v_{AN}. \end{aligned} \tag{9}$$

The presented algorithm is summarized in Fig. 7.

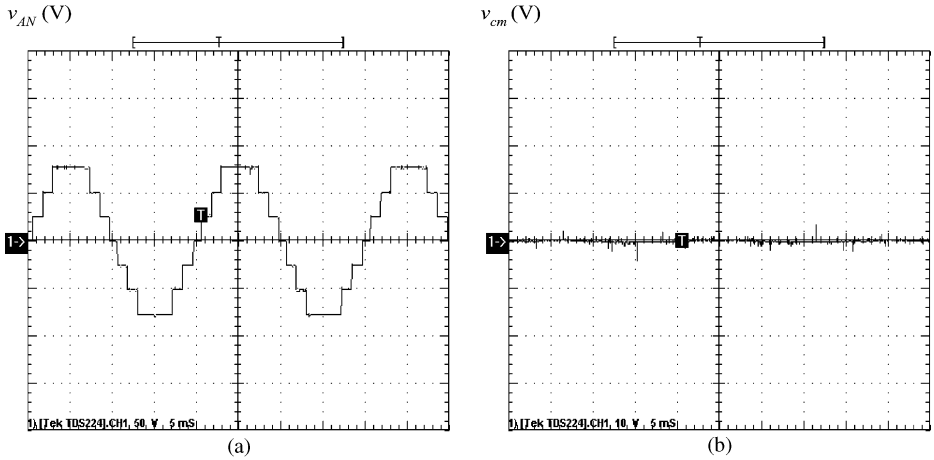

Fig. 8. Seven-level inverter with proposed method (experimental, $m = 0.9$). (a) Output voltage v_{AN} (50 V/div). (b) v_{cm} (10 V/div; time scale: 5 ms/div).

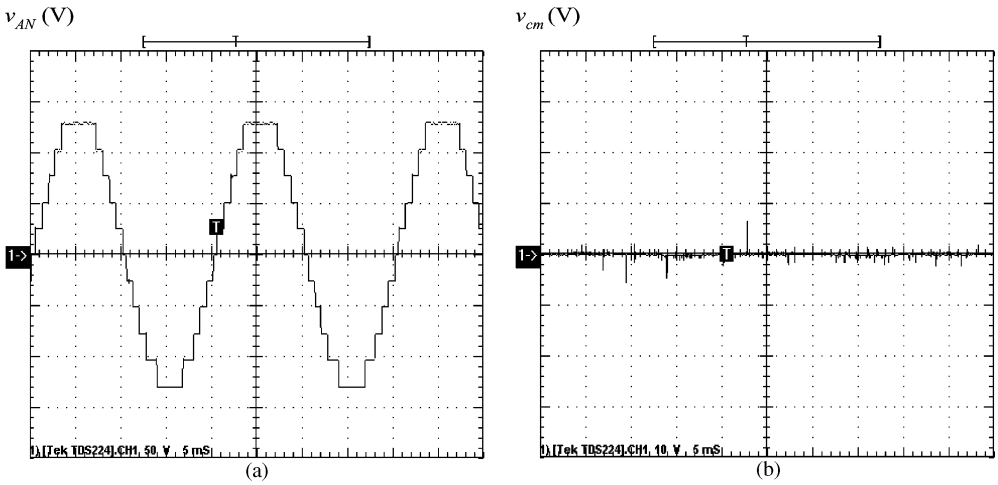

Fig. 9. 11-level inverter with proposed method (experimental, $m = 0.9$). (a) Output voltage v_{AN} (50 V/div). (b) v_{cm} (10 V/div; time scale: 5 ms/div).

VI. Experimental Results

The modulation strategy was applied in a multicell inverter prototype, with three and five cells in each phase. The 16-bit fixed-point digital signal processor (DSP) controller ADMC331 was employed to transform the reference vector and control the inverter to synthesize the appropriate output voltage. In this hardware implementation, the execution time to generate the output voltage was only 6 μs.

Fig. 8(a) represents the phase voltage v_{AN} in a seven-level inverter controlled by the proposed method, operating with a modulation index of $\mathrm{m} = 0.9$ and fundamental frequency of 50 Hz. This result has a similar fundamental voltage to the one originated by the MLSPWM method, shown in Fig. 4. It must be noted that the number of commutations in the load voltage in Fig. 8 is drastically reduced with respect to the voltage of Fig. 4. Fig. 8(b) shows that the proposed method effectively eliminates the common-mode voltage in comparison to the values observed in Fig. 5.

Fig. 9 presents experimental results obtained in a 11-level inverter, which has five cells in series connection per phase. The waveform of Fig. 9(a) corresponds to the output voltage v_{AN} with a modulation index of $m = 0.9$ and an output frequency of 50 Hz. The resulting voltage is highly sinusoidal and the common-mode voltage is also eliminated.

An 11-level inverter has many more voltage vectors to be selected from than a seven-level inverter. However, the number of calculations involved in the algorithm to select a voltage vector is the same for both inverters and, therefore, the execution time does not increase.

VII. Linear Range and THD Analysis

The use of vectors with $v_{cm} = 0$ increases the distance between $\boldsymbol{v}_{\mathbf{ref}}$ and the vectors effectively delivered by the inverter. This means an increase in the error of the generated voltage with respect to the reference.

Fig. 10 represents the relationship between the amplitude of the fundamental load voltage a_1 and the modulation index m, which must be linear for a good modulation method. In this paper, the modulation index is defined as

$$m = \frac{|v_{\mathrm{ref}}| \cdot \sqrt{3}}{2 \cdot C_n \cdot Vcc} \tag{10}$$

where C_n is the cell number in each phase. It can be observed that the proposed method does not have a linear relationship

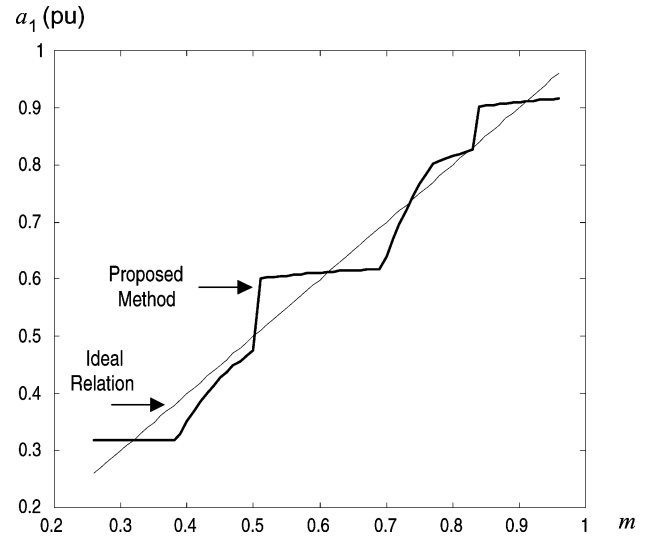

Fig. 10. Fundamental load voltage (a_1) versus modulation index (m) in a seven-level inverter working with the proposed modulation scheme (1 pu $= 6 \cdot Vcc/\sqrt{3}$).

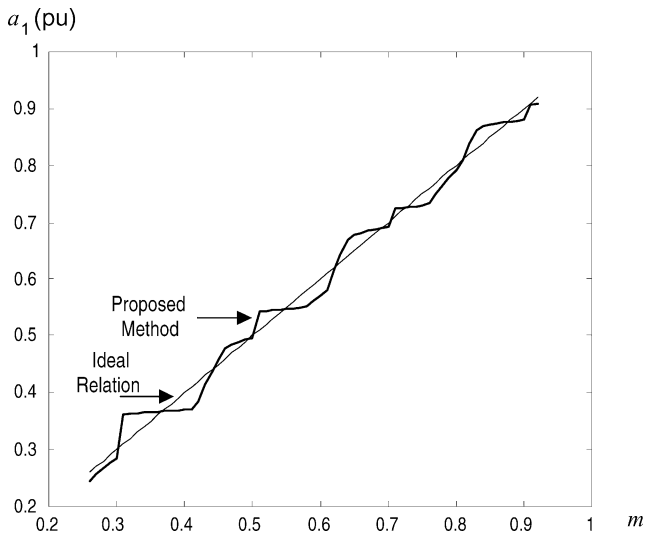

Fig. 11. Fundamental load voltage ($a1$) versus modulation index (m) in an 11-level inverter working with the proposed modulation scheme (1 pu $= 10 \cdot Vcc/\sqrt{3}$).

between a_1 and m, which is not desirable. This fact is a natural result of the reduction in the number of available space vectors. This problem is less severe in inverters with a higher number of levels. Fig. 11 shows that an 11-level inverter has a much better relationship between a_1 and m.

Another important aspect to consider in the evaluation of this modulation method is the total harmonic distortion (THD) of the load voltage. Fig. 12 shows that the THD increases with decreasing modulation index m, which is normal for all modulation methods. This figure also shows that this method has a comparable THD with respect to the MLSPWM strategy. The reason for this effect is that the MLSPWM carrier-based method does not fully utilize the nearest available phase voltage with respect to a sinusoidal reference, whereas the vector method does. However, the performance of the carrier-based PWM method is superior considering the harmonic currents. This is a logical

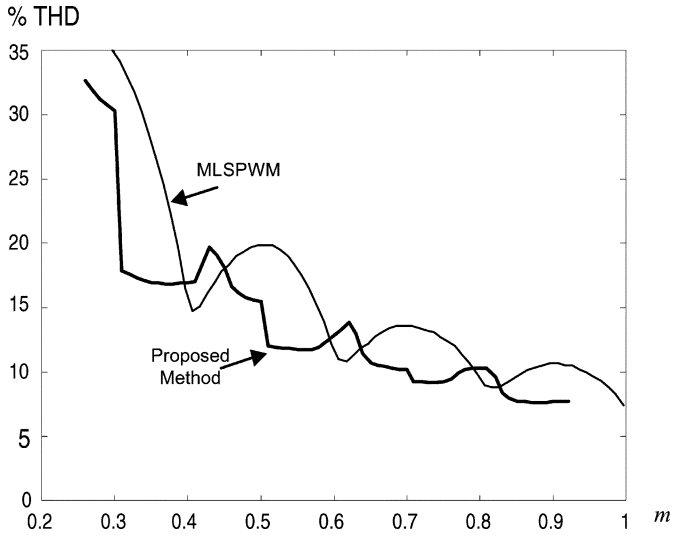

Fig. 12. Load voltage THD comparison in an 11-level inverter for different modulation indexes.

consequence of the low-pass filtering capability of every ac machine drive.

VIII. Conclusion

The classical MLSPWM widely used in industry presents a large amount of commutations in the common-mode voltage, consequently producing a large quantity of current spikes.

The new modulation strategy proposed in this paper eliminates common-mode voltages in multilevel inverters, selecting only space voltage vectors with $v_{cm} = 0$, operating with almost fundamental switching frequency. This method has a comparable voltage THD with respect to the MLSPWM, despite the fact that not all possible vectors are used. The reason for this result is that the space-vector control proposed in this paper selects the nearest voltage vector with respect to a reference.

The authors believe that this method is suitable for inverters with seven or more levels, where the high number of vectors ensures a good approximation of the commanded voltage by a zero common-mode voltage vector. Otherwise, the application of the modulation method in a multilevel inverter with a lower number of levels would generate voltages and currents with high levels of distortion.

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